

REMARKS

The new rejection of Claims 5 to 10 under 35 USC 102 and 103 from the newly cited Huang, et al. patent alone or in combination is inappropriate on the basis of the earlier priority date of the above application and the attested English translation of the priority application filed November 12, 2003. A copy of the postcard receipt for this is attached.

Besides, Huang discloses, in column 5, lines 47 to 51, "The heat sink 43 is integrally formed with an extending portion 431 extending upwardly and outwardly at each longitudinal side edge 430 thereof. This can help enhance the bonding of the heat sink 43 to the encapsulant 46, and provide extra heat dissipating area for improving the heat dissipating efficiency in the condition of no increase in the dimension of the semiconductor package 4." In comparison, the plate of the subject application is a flat plate and is used to expose the overflow adhesive portion so that a testing instrument can detect the size of the overflow adhesive portion and the thickness of the adhesive layer. Thus, the feature of the plate of the subject application is different from that of the heat sink 43 of US 6,650,006. Additionally, the limitation of "the portion of the plate under the second chip is wrapped in the adhesive layer, and the adhesive layer is exposed at the corner formed by the plate and the second chip along the longitudinal side of the plate" of Claims 5 and 6 of the subject application is not disclosed in US 6,650,006. Therefore, US 6,650,006 neither anticipates nor makes obvious Claims 5 and 6 of the application.

The new rejection of Claim 5 under 35 USC 102 for anticipation by the newly cited Nakanishi patent is also traversed. The stacked semiconductor chip package disclosed by Nakanishi (US 6,072,243) comprises a lead frame 10 having a flat-plate-shaped die pad 11, inner leads 12, and outer leads 13. To one surface 11a of the die pad 11 is bonded a first

semiconductor chip by an insulating film 1 which serves as a first adhesive layer, while to the other surface 11b of the die pad 11 is bonded a second semiconductor chip 8 by a silverless paste 2 which serves as a second adhesive layer (FIGs. 1 and 2). In comparison, in the stacked semiconductor chip package of the subject application (FIG. 2C), the first chip 22 is mounted on the substrate 21, the plate 23 is mounted on the first chip 22, the second chip 24 is mounted on the plate 23. The structure of the stacked semiconductor chip package of the subject application is different from that of US 6,072,243. Therefore, US 6,072,243 is not a valid citation to negate the novelty of Claims 5 and 6 of the subject application.

The new rejection of Claims 6 to 10 under 35 USC 102 and 103 from the newly cited Hiraoka, et al. is also traversed on the basis of the priority date of the application and the attested English translation as described above.

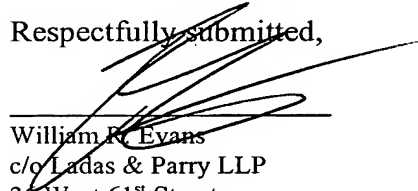
Besides, the plate of the subject application is used to expose the overflow adhesive portion so that a testing instrument can detect the size of the overflow adhesive portion and the thickness of the adhesive layer, which is not disclosed in US 6,740,970. Additionally, the limitation of "the portion of the plate under the second chip is wrapped in the adhesive layer, and the adhesive layer is exposed at the corner formed by the plate and the second chip along the longitudinal side of the plate" of Claims 7 and 8 of the subject application is not disclosed in US 6,740,970 either. Therefore, US 6,740,970 is not a valid citation to negate the novelty of Claims 7 and 8 of the subject application.

The rejection of Claims 6 to 10 from the two newly but doubly wrongly cited Huang, et al. and Hiraoka, et al. patents has already been traversed above.

Besides, "... the portion of the plate under the second chip ... [being] wrapped in the adhesive layer, and the adhesive layer ... [being] exposed at the corner formed by the plate and the second chip along the longitudinal side of the plate ..." is not disclosed or suggested by the combination of these inappropriately cited patents.

Reconsideration and allowance are, therefore, requested.

Respectfully submitted,



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